AMENDMENTS TO THE SPECIFICATION

Please amend paragraph [0001] as follows:

[0001] This application claims priority benefit of U.S. Provisional Patent Application No. 60/498,942 entitled "SYSTEMS AND METHODS INVOLVING DESIGNS," filed August 29, 2003, the disclosure of which is hereby incorporated herein by reference. The present application is related to co-pending and commonly assigned U.S. Patent Application numbers 10/829,843 filed April 22, 2004 ~~[Attorney Docket No. 100204073-1]~~ entitled "SYSTEMS AND METHODS THAT SUPPORT HIERARCHICAL NET NAMING CONVENTIONS USED BY TIMING ANALYSIS TOOLS," 10/29,863 filed April 22, 2004 ~~[Attorney Docket No. 200206536-1]~~ entitled "ADDING NEW NODES INTO AN EXISTING OCCURRENCE MODEL," 10/830,248 filed April 22, 2004 ~~[Attorney Docket No. 200310448-1]~~ entitled "SYSTEMS AND METHODS FOR DELETING OBJECTS IN AN OCCURRENCE MODEL OF A CIRCUIT," ~~filed concurrently herewith,~~ the ~~disclosure~~ disclosures of which [[is]] are hereby incorporated by reference. This application is related to commonly assigned U.S. Patent Application Serial Number 09/709,695 entitled "MEMORY EFFICIENT OCCURRENCE MODEL DESIGN FOR VLSI CAD", filed November 10, 2000, and commonly assigned U.S. Patent Application Serial Number 09/779,965 entitled "METHOD AND APPARATUS FOR TRAVERSING NET CONNECTIVITY THROUGH DESIGN HIERARCHY, filed February 9, 2001, the disclosures of which are hereby incorporated herein by reference.